Amendments to the Specification:

Please replace the abstract of the disclosure at page 31 with the following amended paragraph:

An integrated circuit card <u>includes</u> which includes a circuit for generating a clock signal and for restoring data. The circuit includes a receiver for receiving a radio frequency signal having a pause period; a divider for dividing the received signal; a first counter for counting a period of the divided signal at each non-pause period of the received signal; a second counter for counting a period of the divided signal; and a decoder for generating a synchronous clock signal and a decoded data signal in response to outputs of the first and second counters. The second counter is reset by the synchronous clock signal. The circuit is capable of can generate generating a synchronous clock signal and decode decoding a received data signal so as to be compatible with ISO/IEC 14443 Type A protocol, based on the received radio frequency signal that is transferred from a card reader. The circuit provides an exact decoding result even when the pause period of the received radio frequency received from the card reader varies over a predetermined range.

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